REMARKS

Prior to examination of the above-identified application, please enter this preliminary amendment. No new matter has been added. Applicants respectfully request an action on the merits.

Respectfully submitted,

PILLSBURY WINTHROP LLP

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By: _____
Roger R. Wise
Registration No. 31,204
Attorney for Applicants

725 South Figueroa Street, Suite 2800
Los Angeles, CA 90017-5406
Telephone: (213) 488-7100
Facsimile: (213) 629-1033

APPENDIX

IN THE BACKGROUND:

Please amend the heading on page 1, line 6 as follows:

1. Technical Field [of the Invention]

IN THE SPECIFICATION:

Please amend the paragraph beginning with "The transmitter begins in a high powered," on page 4, line 21, as follows:

The transmitter begins in a high powered, high clock rate mode. High means greater than low. This is illustrated as [step] operation **310** in Figure 3. As shown in [step] operation **320**, the transmitter then invokes the protocol state machine **110** to transmit packets **130** periodically. Starting with raw data, the transmit protocol state machine **110** performs tasks to create packets **130** for transmission, such as dividing the raw data into packets **130**, adding protocol headers, and computing checksums. The transmit protocol state machine **110** sends these packets **130**, as shown in [step] operation **330**, and waits for acknowledgments from the receiver protocol state machine **120**. While waiting, the transmitter protocol state machine **110** switches into a low power, low clock rate mode, as illustrated in [step] operation **340**. While waiting, the transmitter protocol state machine **110** does not wake up to handle every incoming acknowledgment. Instead, it wakes up only when a timer sounds or when an incoming packet buffer reaches a low water mark, as shown in [step] operation **350**. The transmitter then prepares for the sending of additional packets **130**.

Please amend the paragraph beginning with "The receiver protocol machine **120**, in

contrast," on page 5, line 9, as follows:

The receiver protocol state machine **120**, in contrast, starts in a low power, low clock rate mode, as shown in [step] operation **410** of Figure 4. When packets **130** are received from the data communication network **140**, they are simply buffered, as illustrated in [step] operation **420**. [Step] Operation **430** examines whether a buffer has reached a maximum capacity or a high water mark. If such a threshold has not been reached, the receiver protocol state machine **120** returns to [step] operation **410**. When the buffer is full or reaches a high water mark, the receiver protocol state machine **120** is invoked, as illustrated in [step] operation **450**, after switching to a higher powered, higher clock rate mode, as shown in [step] operation **440**. In this scenario, the frequency and power level of the processor is driven by the received or transmitted data. The packets **130** are processed by the receiver protocol state machine **120**, and acknowledgments are sent to the transmitter protocol state machine **110**, if required by the state machine. When the processing of packets **130** is complete, the receiver protocol state machine **120** returns to an idle state, as depicted in [step] operation **410**. The use of buffers and timers in both the transmitter protocol state machine **110** and the receiver protocol state machine **120** results in periodic patterns in data reception and transmission. The periodicity may then be used to manage the power and frequency settings of the host processor.

Please amend the paragraph beginning with "While the above description refers to" on page 7, line 19, as follows:

While the above description refers to particular embodiments of the present invention, it will be understood to those of ordinary skill in the art that modifications may be made without departing from the spirit thereof. The accompanying claims are intended to cover any such

modifications as would fall within the true scope and spirit of the embodiments of the present invention.

Please amend the paragraph beginning with "The presently disclosed embodiments" on page 7, line 23 as follows:

The presently disclosed embodiments are therefore to be considered in all respects as illustrative and not restrictive; the scope of the embodiments of the invention being indicated by the appended claims, rather than the foregoing description. All changes that come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

IN THE CLAIMS:

Please amend claims 12 through 22 as follows:

12. (Amended) [A system to manage energy usage of a processor using at least one protocol state machine comprising a computer readable medium and a computer readable program code stored on the computer readable medium having instructions to:] An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

[send] sending a data packet over a data communication network to a receiver protocol state machine that stores the data packet in an application buffer;

[wait] waiting for an acknowledgment of receipt of the data packet from the receiver protocol state machine; and

[arrange] arranging for a transmission of additional data packets.

13. (Amended) The [system] article of claim 12, wherein instructions are provided to a transmitter protocol state machine to send the data packet while in a high power, high clock rate mode.

14. (Amended) The [system] article of claim 13, wherein instructions are provided to the transmitter protocol state machine to enter an idle low power, low clock rate mode upon completion of data packet transmission.

15. (Amended) The [system] article of claim 14, wherein instructions are provided to the transmitter protocol state machine to return to a high power, high clock rate mode upon a sounding of a timer.

16. (Amended) The [system] article of claim 12, wherein an application buffer and a timer cause periodic patterns in data packet transmission, which are used to manage power and frequency of a processor.

17. (Amended) [A system to manage energy usage of a processor using at least one protocol state machine comprising a computer readable medium and a computer readable program code stored on the computer readable medium having instructions to:] An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

[receive] receiving a data packet from a transmitter protocol state machine over a data

communication network;

[deposit] depositing the data packet in an application buffer;

[process] processing and [verify] verifying the data packet; and

[transmit] transmitting an acknowledgment of receipt of the data packet to the transmitter protocol state machine, wherein the transmitter protocol state machine prepares for transmission of additional data packets.

18. (Amended) The [system] article of claim 17, wherein instructions are provided to a receiver protocol state machine to obtain delivery of the data packet, to store the data packet in the application buffer, to process the data packet, and to send the acknowledgment of receipt of the data packet.

19. (Amended) The [system] article of claim 18, wherein instructions are provided to the receiver protocol state machine to enter an idle low power, low clock rate mode upon obtaining delivery of the data packet.

20. (Amended) The [system] article of claim 19, wherein instructions are provided to the receiver protocol state machine to enter a high power, high clock rate mode when the application buffer reaches a maximum capacity.

21. (Amended) The [system] article of claim 17, wherein the application buffer and a timer cause periodic patterns in data packet reception, which are used to manage power and frequency of a processor.

22. (Amended) The [system] article of claim 17, wherein the data communication network includes at least one of the Internet and an Intranet.